Interrupts

Peter J. Denning

What are Interrupts?

- Normal execution of process may be interrupted by events beyond its control
  - Errors – conditions **inside** the computation that invalidate it
  - External signals –conditions **outside** that require immediate attention

- Called Exceptional Conditions
  - Exception – the act of responding to an exceptional condition
  - Interrupt – the signal from a sensor telling the OS to take an exception

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Examples

- Errors
  - divide by zero
  - overflow
  - array index out of bounds
  - memory protection violation
- External signals
  - time slice end
  - page fault
  - disk completion
  - microkernel system call
  - keyboard
  - packet arrival

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Architecture (1)

- **Sensors** – hardware that detects an exceptional condition
  - divide by zero -- detected in ALU
  - Overflow – detected in ALU
  - array index out of bounds – detected by MMU
  - memory protection violation – detected by MMU
  - time slide end – detected by timer in CPU
  - disk completion – detected by the disk controller
  - microkernel system call – detected in CPU by instruction decoder
  - Keyboard – detected when key is pressed
  - packet arrival – detected by the network card

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Architecture (2)

- **Selector** – Circuit in the CPU that receives signals from all sensors and selects the signal of highest priority
  - Conditions numbered 0,1,2,…,S-1 (S=16 is common) with 0 the highest priority and S-1 the lowest
  - If signals i and j are both on, with i<j, selector chooses i and defers j
  - Remembers deferred signals until they are selected and dispatched
  - When sensor i is selected, selector outputs the code sel=i and sets the interrupt ready bit irdy=1
- **Interrupt check** – a step in each CPU fetch-execute cycle to see if irdy=1. If so, jump the CPU to run the dispatcher while turning off interrupts and entering kernel mode.

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Architecture (3)

- **Dispatcher** – a short software routine that sets up activation record (AR) for the proper interrupt handler (IH) software and calls it.

- **Handling** –IH executes its function, completes with RET (return) instruction, which pops the AR from the stack and restores execution of the process originally interrupted. Most handlers turn interrupts back on, so that higher priority interrupts can take precedence and interrupt them.

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Architecture (4)

- **Mask (priority indicator)** – A code indicating which of incoming sensor signals the selector should act on. Corresponds to the priority of the handler. Hides pending interrupt signals from sensors of lower priority than the executing handler.
  - Typically mask has S bits of the form prefix of 1s followed by suffix of 0s
  - When no interrupts are being handled, mask is all 1s (all sensors enabled)
  - User code operates with the all-1s mask
  - Example: Handler for sensor 3 has mask 111000000000000 meaning sensors 0, 1, 2, are enabled and all others ignored
  - Mask stored in the PSW of the CPU

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Architecture (5)

- **Interrupt Argument (arg**) – a code generated by selector to be passed as a parameter to the handler
  - for example, the virtual address causing a page fault interrupt
  - or, a code indicating which kernel routine targeted by system call

- **Interrupt Vector (IV)** – list of entry points for IHs; stored in kernel memory

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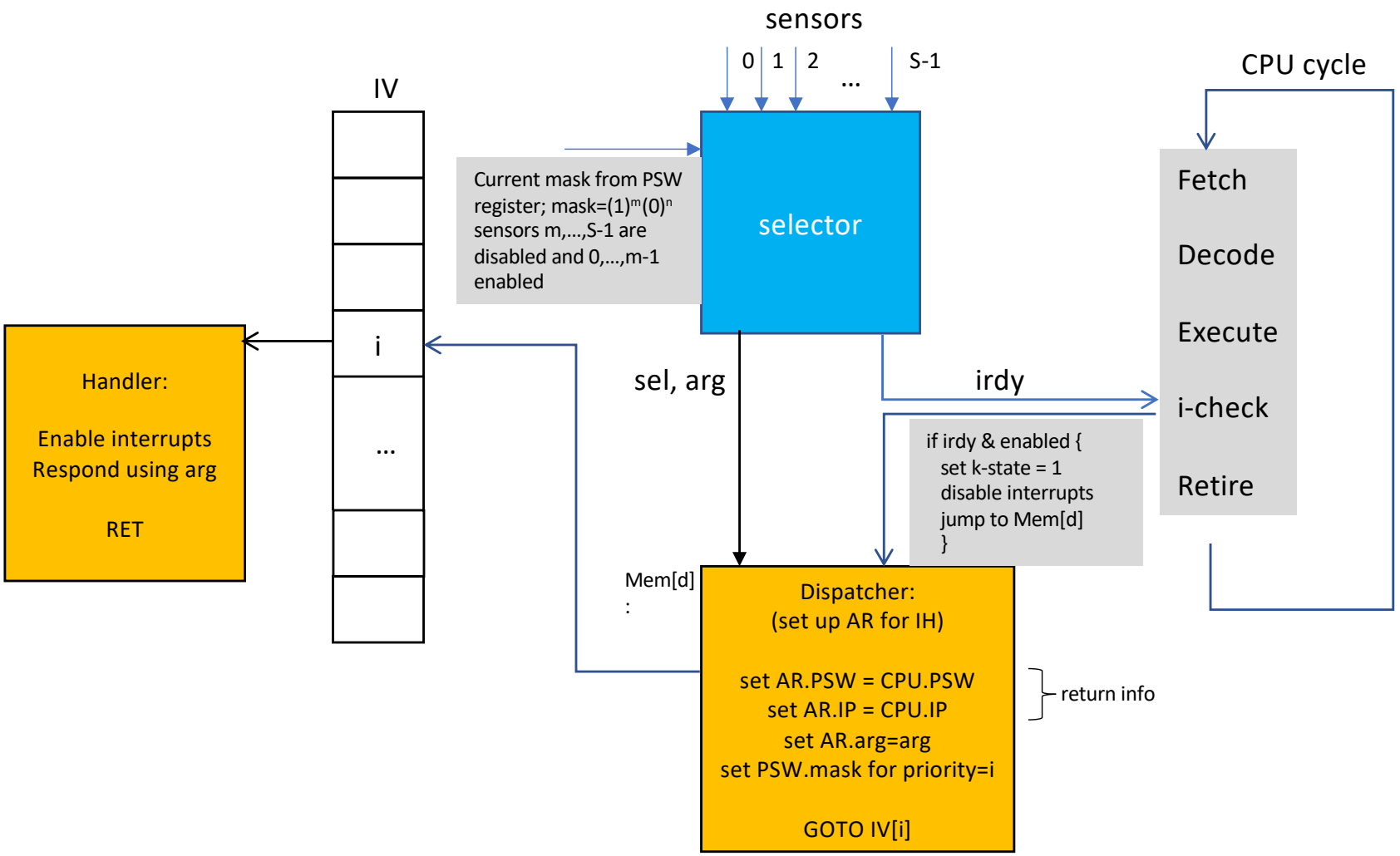

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Kernel call – Microkernel

- Micro kernel routines require extra security – they are run in kernel model and have access to all of kernel memory
- Micro kernel routines, and only those routines, run in kernel mode
- Force entry to kernel routine at its entry point (protected entry)
- Let Ek = memory address of first instruction of a kernel routine k
- Ordinary CALL Ek not allowed because user could change Ek to something else
- Instead create kernel vector with KV[k] = Ek meaning that kernel routine with ID code k has entry point Ek. KV private in kernel space.
- Instruction KC k implements “CALL KV[k]”

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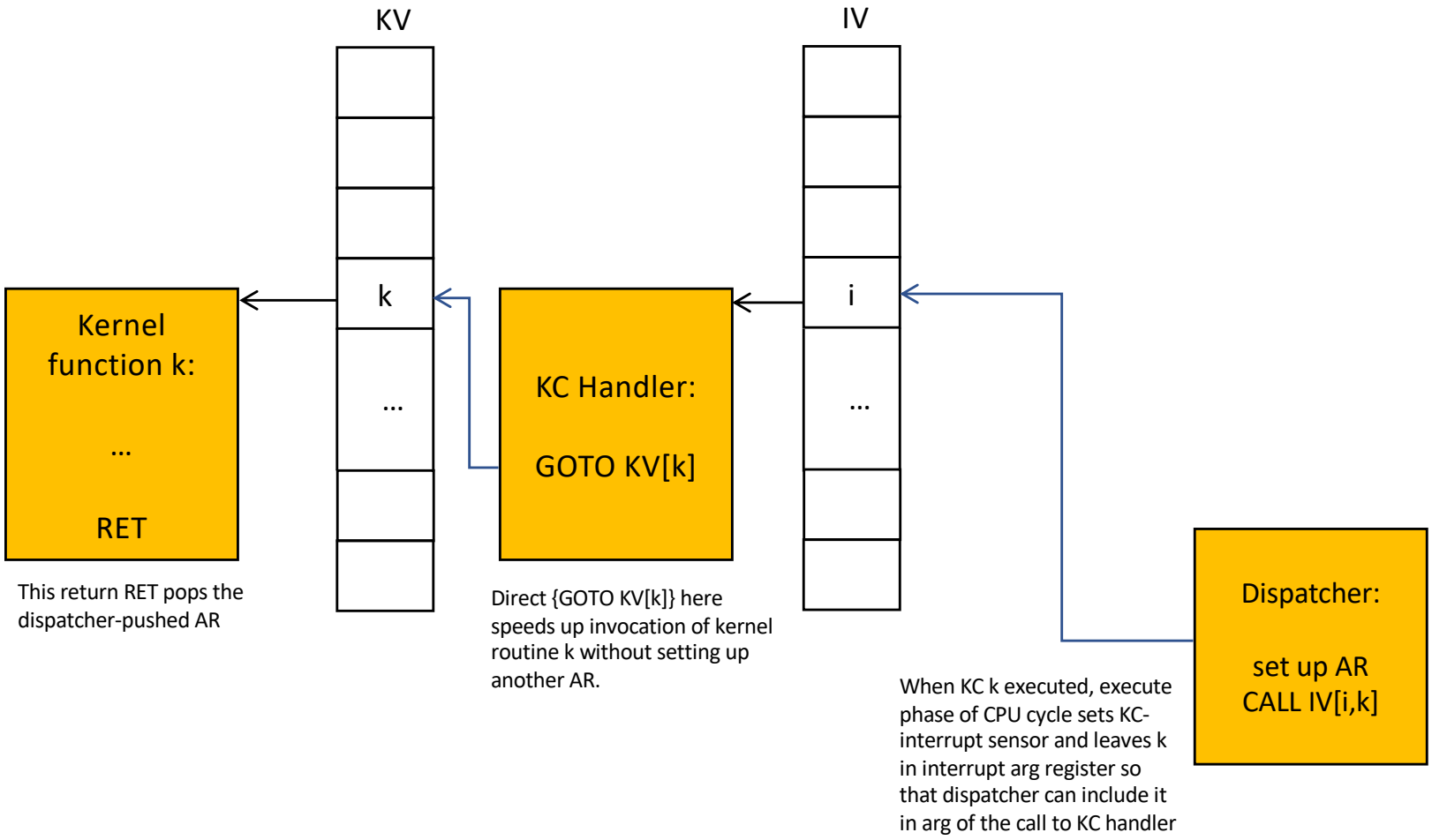

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ORDER OF INTERRUPT PRIORITIES

- Priorities of interrupts are design decisions set by negotiation between software and hardware engineers
- However, they are not arbitrary.
- Generally, interrupts for events internal to a process take priority over those that can switch context (KC, TSE).
  - Reason: if KC/TSE is higher priority than interrupt k, k will be deferred until after the KC/TSE is complete, and the new process will see interrupt k. If interrupt k is internal to the previous process, it will be spurious in the new process.
- All interrupts resulting from events external to a process are lower priority than KC/TSE.

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Supervisor call – User kernel

- User kernel routines run in user mode. Therefore there is no need to use the KC instruction to enter them.
  - In this case, the entry points of the user kernel API can be made available to the compiler, which can use ordinary procedure calls for them.
- Some operating systems use protected entry for user kernel as well as micro kernel, as added protection against malware.
  - In this case, the system would be set up to use KC for all kernel calls.

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